IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Wachtmann	Atty. Docket:	2550/185
Serial No.:	10/670,673	Art Unit:	2814
Filing Date:	September 25, 2003	Examiner:	Pizarro Crespo, Marcos D
Invention:	METHOD OF FORMING A SURFACE MICROMACHINED MEMS DEVICE		

Mail Stop Appeal Brief-Patents
Commissioner for Patents
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APPEAL BRIEF

Applicant submits this appeal brief for the above captioned application.

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Real Party in Interest

Analog Devices, Inc.

Related Appeals and Interferences

None.

Status of Claims

Applicant appeals the final rejection of claims 1, 3-5, 7-8 and 15-19, which are pending in the application. Claims 9-14 and 20 stand withdrawn.

Status of Amendments

No amendment subsequent to the final rejection has been entered.

Summary of Claimed Subject Matter

Note: all page and line references, except as noted, refer to the above-captioned U.S. patent application, no. 10/670,673.

The method of Claim 1 forms a surface micromachined MEMS device that has no semiconductor junctions between its substrate and conductive paths (fig. 2, generally.) A substrate is provided and an oxide is applied on the substrate. (P. 6, lines 18-19; fig. 2, **200;** fig. 3, **22, 12**). A conductive path is deposited directly on the oxide. (P. 7, lines 8-9; fig. 2, **202**; fig. 4, **24, 22**).The conductive path is capable of transmitting electronic signals between two points of the MEMS device (p. 9, lines 20-21.) Circuitry (p. 5, lines 24-25; fig. 8, **18)** and structure (fig. 2, **210;** p. 9, lines 3-8; fig. 8, **32)** are formed, where the circuitry and structure are the two points. The oxide spaces the conductive path from the substrate, forming a MEMS device free of semiconductor junctions formed by the substrate and the conductive path. (P. 7, lines 12-15; fig. 4, **24, 22.**) The conductive path between the circuitry and the structure is then connected. (P. 10, lines 10-12; figs. 1, 8, **20)**

The method of Claim 15 forms a sensor (fig. 2, generally.) An oxide is formed on a substantially intrinsic semiconductor substrate. (P. 6, lines 18-22; fig. 2, **200;** fig. 3**, 22, 12**). A conductive path is formed directly on the oxide. (P. 7, lines 18-19; fig. 2, **202**; fig. 4, **24, 22**). The oxide and the conductive layer are formed by surface micromachining processes (p. 6, lines 15-22) with the oxide electrically isolating the conductive path from the substrate. Circuitry (p. 5, lines 24-25; fig. 8, **18)** and structure (fig. 2, **210;** p. 9, lines 3-8; fig. 8, **32)** are formed. A conductive path is connected between the circuitry and the structure (p. 10, lines 10-12; figs. 1, 8, **20)**, such that the conductive path is capable of transmitting an electronic signal between the circuitry and the structure (p. 9, lines 20-21.)

The method of Claim 19 further defines the spacing of the oxide layer in Claim 15 as between about 0.15 microns and 1.5 microns. (P. 6, lines 23-24.)

Grounds of Rejection to be Reviewed on Appeal

The rejections involved in this appeal are:

1) Claims 1, 3-5, 7-8, and 15-18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Montague (U.S. pat. no. 5,798,283) in view of Kim (U.S. pat. no. 6,500,763) or Lee (U.S. pat. no. 6,160,314).
2) Claim 19 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Montague/Kim/Lee in view of Fladre (U.S. pat. appl. no. 200410152272).

Argument

Issue 1: Rejection of Claims 1, 3-5, 7-8, and 15-18 under 35 U.S.C. § 103(a) as being unpatentable over Montague (U.S. pat. no. 5,798,283) in view of Kim (U.S. pat. no. 6,500,763) or Lee (U.S. pat. no. 6,160,314).

As will be shown below, these rejections for obviousness must fail because a prima facie case of obviousness has not been made for any of the pending claims of the subject application. No convincing motivation or suggestion to combine either of the secondary references (Kim/Lee) with the primary reference (Montague) to achieve the claimed embodiments of the invention has been shown.

Claim 1 of the subject application is directed to a method of forming a surface micromachined MEMS device having both circuitry and structure. Among other things, Claim 1 requires "depositing a conductive path directly on an oxide" that was applied to a semiconductor substrate. This conductive path connects between the circuitry and structure. In contrast, Montague '283 does not teach such a process. Instead, the Montague reference teaches depositing polysilicon on a silicon nitride insulating layer. In particular, as shown in fig. 1 and col. 6, lines 8-13 of Montague, Montague's MEMS device has a doped polysilicon layer 24 (a conductive path) on a silicon nitride layer 22.

To provide a motivation or a suggestion to replace Montague's nitride layer 22 with an oxide layer, a reference would need to teach or suggest that a nitride layer and an oxide layer are fully equivalent in an application such as the insulating layer 22 in Montague's device. Lee '314 never teaches or suggests that nitride and oxide are interchangeable substitutes when used as a singular insulating

layer over a semiconductor substrate. Therefore, there is no suggestion or motivation to combine Lee '314 with Montague to achieve the embodiment of Claim 1. The details are provided below.

Lee '314 teaches the use of a complex structure as a polishing stop for fabricating a semiconductor device. This structure is shown in fig. 2A of Lee:

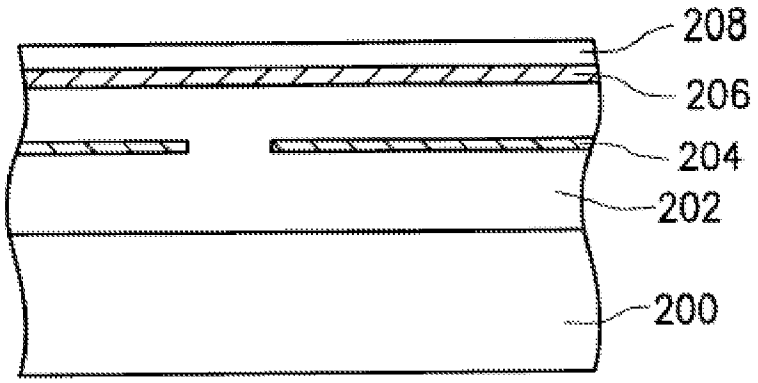

FIG. 2A

Lee describes the structure thusly:

"Referring first to FIG. 2A, a first dielectric layer 202 is formed on a semiconductor substrate 200. The dielectric layer 202, for example, is a silicon dioxide layer. An etching stop layer 204, for example, a silicon nitride layer, is formed in the dielectric layer 202. The materials of the polishing stop layer 206 and the dielectric layer 202 are different. A polishing stop layer 206 is formed on the dielectric layer 202. The material

> of the polishing stop layer 206 is, for example, silicon-oxy-nitride, silicon nitride or aluminum oxide, which are not easily removed by CMP and have a high polishing selectivity. The dielectric layer 202 is therefore more easily removed by chemical mechanical polishing than the polishing stop layer 206. A second dielectric layer 208 is formed on the polishing stop layer 206. The material of the second dielectric layer is different from the polishing stop layer 206, for example, silicon dioxide." See Lee '314, col. 2, lines 47 to 62.

A prima facie case of obviousness requires, *inter alia*, some teaching, suggestion, or motivation to combine the cited references. See, e.g., *In re Kahn*, 441 F.3d 977, 986 (Fed. Cir. 2006); MPEP 2143.01. To provide a motivation or a suggestion to replace Montague's nitride layer 22 with an oxide layer, a reference would need to teach or suggest that the materials are <u>fully</u> equivalent in an application such as the insulating layer 22 in Montague's device. Lee never describes nitride and oxide as interchangeable substitutes when used as a singular insulating layer over a semiconductor substrate. This is the function performed by Montague's insulating layer 22. Instead, Lee mentions that in the polishing stop layer of the complex sandwich shown in fig. 2A (layer 206), one or more materials would work.

Performance as a polishing stop is but one attribute of Montague's silicon nitride insulating layer 22. For example, Montague states that "the remainder of the nitride layer 22 covering the inner surfaces of each cavity **20** will <u>serve as a dielectric isolation layer and also as an etch stop layer</u> during process steps for patterning a first sacrificial layer 30" (see, Montague, column 5, lines 42-44.). Further, Montague states:

> "After planarization of the substrate, a second nitride layer (i.e. a cap layer) 34 may be deposited over the planar upper surface of the substrate covering the remaining portion of the first nitride layer 22 and any exposed portions

> of the sacrificial layers 30 and 32. thereby forming a nitride-to-nitride seal for sealing the encapsulated MEM devices." (See, Montague, column 7, lines 17-22, emphasis added)

A reference would need to teach or suggest equivalence of all pertinent properties of an oxide for the silicon nitride layer 22 in Montague's application to provide a suggestion to replace nitride with oxide – such properties include the dielectric constant of the material, the ability to form a seal with Montague's cap layer 34, the ability to serve as an etch stop, etc. Lee '314 lacks such a teaching. Further, Montague effectively teaches away from using an oxide layer for the silicon nitride 22 layer, since the silicon nitride layer is already formed on a thin oxide layer. If silicon dioxide were a suitable substitute for the nitride layer in Montague's device, Montague could have used a single, thicker layer of silicon dioxide in place of the more complex nitride on silicon dioxide layers in the device Montague described.

Since Lee does not teach that oxide and nitride have fully equivalent properties for the attributes of Montague's nitride insulating layer 22, a suggestion or motivation to combine Lee' '314 teachings with Montague's teaching is lacking and a prima facie case of obviousness has not been made. Therefore, Claim 1 is deemed non-obvious over Montague in view of Lee.

Likewise, Kim '763 never teaches or suggests that nitride and oxide are interchangeable substitutes when used as a singular insulating layer over a semiconductor substrate. Therefore, there is no suggestion or motivation to combine Kim '763 with Montague to achieve the embodiment of Claim 1. The details are provided below.

Kim '763 teaches a method for manufacturing an electrode of a capacitor.

FIG. 1

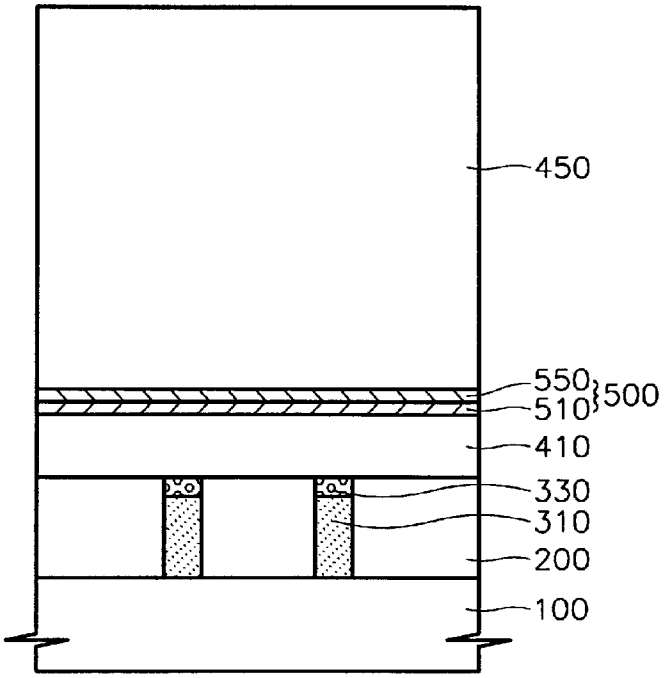

Fig. 1 of Kim '763 shows the structure formed by Kim's process. Kim describes the process, thus:

"In a first embodiment of the present invention, FIG. 1 schematically illustrates a process of forming an etch stop layer 500 and a mold sacrificial insulating layer 450 on a **semiconductor substrate 100**. More specifically, a conductive plug 310, which will be electrically connected to a storage node, is formed on the semiconductor substrate 100 using a standard buried contact process. The conductive plug 310 is surrounded by a lower insulating layer 200 so that the **conductive plug 310** may be insulated from other conductive patterns (not shown) such as gates, which are formed on the semiconductor substrate 100, while the conductive plug 310 is electrically connected to an active region in the semiconductor substrate 100. Put another way, the conductive plug 310 functions as a buried contact. The thickness of the lower insulating layer 200 varies with necessity, but may be about 4000-5000 .ANG. depending on the thickness of the conductive plug 310.

The conductive plug 310 may be formed of various conductive materials, for

example, conductive polysilicon. The conductive plug may be covered with a diffusion barrier layer 330. The diffusion barrier layer 330 may include an ohmic layer to serve as an ohmic contact.

On the semiconductor substrate 100 having topology as a result of forming such various patterns, a support insulating layer 410 is formed. The support insulating layer 410 serves to support a three-dimensional storage node so that the storage node does not fall down or collapse. The support insulating layer 410 may be formed of an insulating material, which is usually used when a semiconductor device is manufactured. For example, the support insulating layer 410 may be formed by depositing a silicon oxide (SiO.sub.2) layer on the lower insulating layer 200 such that the conductive plug 310 is covered with the silicon oxide layer. The support insulating layer 410 must be formed to at least a minimum thickness for supporting a storage node. It is preferable that the support insulating layer 410 is formed to a thickness of about 2000-3000 .ANG.

Thereafter, the **etch stop layer 500**, which will be used in a later etching process, is formed on the support insulating layer 410. In one embodiment of the present invention, the etch stop layer 500 includes a tantalum oxide layer 510. For example, the tantalum oxide layer 510 is formed of ditantalum pentaoxide (Ta.sub.2 O.sub.5) on the support insulating layer 410 by sputtering or chemical vapor deposition (CVD). The tantalum oxide layer 510 is preferably formed to at least the minimum thickness needed to stop etching. For example, the thickness of the tantalum layer 510 may be about 10-90 .ANG., but may vary depending on a later etching process." See Kim '763, col. 3, line 31 to col. 4, line 19, emphasis added.

Thus, in Kim '763, conductor 310 lies between substrate 100 and the etch stop layer 500. While Kim may teach that in Kim's specific complex semiconductor structure, an etch stop layer may either be a nitride or an oxide, one skilled in this art could not infer from this teaching that Montague's insulating layer 22 could equally well be either a nitride or an oxide. Montague's insulating layer 22 lies between the conductive path and the substrate and, as described above, serves additional functions as compared to Kim's etch stop layer 500, i.e., insulating layer, sealant in combination with a superimposed nitride layer, polishing stop, etc. Equivalence of materials can only be inferred from consideration of all relevant properties of the materials. Kim '763 like Lee '314

cannot serve as motivation or a suggestion to replace Montague's insulating layer with an "all oxide" layer since there is no teaching in Kim that the oxide would perform equally well or better than the nitride in Montague's device structure.

Since Kim '763 does not teach that oxide and nitride have fully equivalent properties for the attributes of Montague's nitride insulating layer 22, a suggestion or motivation to combine Kim '763 teachings with Montague's teaching is lacking and a prima facie case of obviousness has not been made. Therefore, Claim 1 is deemed non-obvious over Montague in view of Kim.

Since Claim 1 is allowable over the cited art, claims 3-5, 7 and 8, which depend from Claim 1 and add further limitations are also allowable for at least the same reasons as for Claim 1.

Claim 15, like Claim 1, requires, in part:

"…forming a conductive path directly on the oxide, …, the oxide electrically isolating the conductive path from the substrate."

Thus, Claim 15 and Claims 16-18, which depend from Claim 15 and add further limitations, are also allowable for the same reasons as for Claim 1.

Issue 2: Rejection of Claim 19 under 35 U.S.C. 103(a) as being unpatentable over Montague/Kim/Lee in view of Fladre (U.S. pat. appl. no. 200410152272).

The rejection for obviousness relies on Montague/Kim/Lee for teaching the limitations of Claim 15, from which Claim 19 depends. As described above, no motivation or suggestion has been shown to combine either of the secondary references, Kim and Lee, with the primary reference, Montague, to achieve the embodiment of Claim 15. Fladre, likewise, does not provide the teaching, suggestion or motivation, lacking in Montague/Kim/Lee, to combine Montague and Kim or Lee to achieve the embodiment of Claim 15. Since neither Montague/Kim/Lee nor Fladre provides a suggestion or motivation to combine these references, a prima facie case of obviousness has not been made. Thus, Claim 19 is deemed non-obvious over Montague/Kim/Lee in view of Fladre.

For all the foregoing reasons, Applicant submits that all pending claims in the application are allowable over the art of record and early notice to that effect is respectfully solicited.

Respectfully submitted,

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Claims Appendix

Application Serial No. 09/670,673

1. A method of forming a surface micromachined MEMS device, the method comprising:

providing a substrate;

applying an oxide on the substrate;

depositing a conductive path directly on the oxide, the conductive path being capable of transmitting an electronic signal between two points on the MEMS device, the oxide spacing the conductive path from the substrate, the MEMS device being free of semiconductor junctions formed by the substrate and the conductive path,

forming circuitry and structure, the circuitry and structure being the two points; and

connecting the conductive path between the circuitry and the structure.

3. The method as defined by Claim 1 wherein the structure is electrically isolated from the substrate.

4. The method as defined by Claim 1 further comprising:

applying an additional insulator above the conductive path;

depositing an additional conductive path to the additional insulator, the conductive path and the additional conductive path being in different planes of the MEMS device.

5. The method as defined by claim 4 further comprising electrically connecting the conductive path and additional conductive path with a connector, the connector being one of a via and a staple.

7. The method as defined by Claim 1 wherein the substrate is free of embedded electrodes.

8. The method as defined by Claim 1 wherein the conductive path comprises polysilicon.

15. A method of forming a sensor, the method comprising:

forming an oxide on a substantially intrinsic semiconductor substrate;

forming a conductive path directly on the oxide, the oxide being formed and the conductive layer being formed by surface micromachining processes, the oxide electrically isolating the conductive path from the substrate;

forming circuitry and structure; and

connecting the conductive path between the circuitry and the structure, the conductive path being capable of transmitting an electronic signal between the circuitry and the structure.

16. The method as defined by Claim 15 wherein the structure is electrically isolated from the substrate.

17. The method as defined by Claim 15 wherein the MEMS device is free of semiconductor junctions formed by the substrate and the conductive path.

18. The method as defined by Claim 15 further comprising:

applying an additional insulator above the conductive path; and

depositing an additional conductive path to the additional insulator, the additional conductive path and the conductive path being in different planes of the MEMS device.

19. The method as defined by Claim 15 wherein the oxide has a thickness that spaces the substrate and conductive path to a given spacing, the given spacing being between about 0.15 microns and 1.5 microns.

Evidence Appendix

None

Related Proceedings Appendix

None.

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